REMARKS

The foregoing claim amendments amend claims 1, 10 and 19. Now in the application are Claims 1-20 of which Claims 1, 10, and 19 are independent. The following remarks address all stated grounds for rejection, and Applicants respectfully submit that the presently pending claims, as identified above, are in condition for allowance.

Claim Amendments

Applicants have amended claims 1, 10 and 19 to clarify the scope of claimed invention. In particular, claims 1, 10 and 19 have been amended to claify the meanings of the claim languages. Claims 1, 10 and 19 have also been amended to remove the claim languages added in the previous claim amendment, as suggested by the Examiner. No new matter has been introduced. Applicants therefore submit that the claim amendments should be entered and considered.

Objection to the Drawings

The drawings are objected to for minor informalities. Applicants have amended the drawings to correct the informalities. In light of the amendments to the drawings, Applicants request the Examiner to reconsider and withdraw the objection to the drawings.

Claim Objections

Claim 1 is objected to under 35. U.S.C. 112, second paragraph, as being indefinite. In particular, the Examiner notes in the Office Action that it is unclear how an assignment of a register is assigned as a destination operand in the last paragraph of claim 1. Applicants have amended claim 1 to remove the words added in the previous claim amendments. In light of the claim amendments, Applicants respectfully request the Examiner to reconsider and withdraw the claim objection to claim 1.

Claim Rejections - 35 U.S.C. § 102

Claims 1-3, 5, 7-8, 10-12, 14, 17 and 19 are rejected under 35 U.S.C. § 102(b) as being anticipated by European Patent Application Publication No. 0 600 611 A2 ("Faraydon"). Applicants respectfully traverse this rejection for the following reasons.

Independent claim 1 is directed to a method for managing a number of physical registers in a microprocessor. The method provides a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. The method further includes the step of storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The physical register assignment of the selected physical register is transferred from the second structure to a third structure after retirement of the selected instruction. *When the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure*. Claim 10 is another method claim reciting similar limitations and claim 19 is a medium claim that parallels claim 1.

Applicants respectfully submit that the cited prior art reference fails to disclose each and every element of the claimed invention. Applicants submit that Faraydon fails to disclose that *when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure*, as recited in claims 1, 10 and 19.

The Examiner notes in the Office Action that general purpose registers (GPR) (16) associated lock bits (17), collision vector tables (CVT) (11), and Rename 2 (18) disclosed in the Faraydon reference correspond to the first, second and third structures of the claimed invention, respectively, and hence anticipate the claimed invention. Applicants respectfully disagree.

In the Faraydon reference, logical or architectural registers, such as registers R0-R3, are assigned to GPR as destination operands for the fetched instructions. The Faraydon reference

discloses that Rename 2 (18) receives new physical locations of GPR (16) used as destination operands in the execution of the fetched instructions after the fetched instructions are executed. When Rename 2 is updated with new physical locations of GPR, the old physical locations of GPR are returned to CVT (11). For example, as depicted in Fig. 12 of the Faraydon reference, Rename 2 receives new physical location 04 for R3 and returns the old physical location 03 for R3 to CVT 00 after the first instruction (R3 ← R1 + R2) is executed. (*See*, Faraydon, Fig. 12, dotted arrows). For another example, in Fig. 23a of the Faraydon reference, Rename 2 receives new physical location 09 for R3 and the old physical location 04 for R3 is returned to CVT 11 after the instruction (R3 ← R2*R0) is executed.

In contrast, the claimed invention transfers information identifying the selected physical register as available from the third structure to the first structure when the architectural register is assigned as a destination operand for a subsequent instruction. In the Faraydon reference, the control word generator (9) assigns the logical or architectural registers, such as registers R0-R3, to GPR as destination operands for the fetched instructions. When the architectural registers are assigned to GPR in the Faraydon reference, Name 1 (12) is updated with the assignment of GPR, and Name 2 is not affected and does not transfer any information identifying GPR as available. Name 2 is updated with the assignment of GPR used in the execution of the fetched instruction and returns the old physical locations of GPR to CVT after the fetched instructions are executed. Moreover, Name 2 returns the old physical locations of GPR to CVT, not to GPR, which is indicated by the Examiner to correspond to the first structure of the claimed invention. The Faraydon reference does not disclose that when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from Rename 2 to GPR.

In light of the arguments set forth above, Applicants submit that the Faraydon reference fails to disclose each and every element of claims 1, 10 and 19. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 1-3, 5, 7-8, 10-12, 14, 17 and 19 under 35 U.S.C. §102(b).

Claim Rejections - 35 U.S.C. § 103

Claims 4, 13 and 20 are rejected under 35 U.S.C. § 103(a) as unpatentable over Faraydon. Applicants respectfully traverse the rejection for the following reasons.

Claim 4, 13 and 20 depend on independent claims 1, 10 and 19, respectively. Applicants respectfully submit that the cited prior art reference fails to teach or suggest all of the limitations of independent claims 1, 10 and 19. Applicants submit that Faraydon fails to teach that *when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure*, as recited in claims 1, 10 and 19.

Faraydon teaches that the control word generator (9) assigns architectural registers, such as registers R0-R3, to GPR as destination operands for the fetched instructions. When the architectural registers are assigned to GPR in the Faraydon reference, Name 1 (12) is updated with the assignment of GPR, and Name 2 is not affected and does not transfer any information identifying GPR as available. Name 2 is updated with the assignment of GPR used in the execution of the fetched instruction and returns the old physical locations of GPR to CVT after the fetched instructions are executed. Moreover, Name 2 returns the old physical locations of GPR to CVT, not to GPR, which is indicated by the Examiner to correspond to the first structure of the claimed invention. The Faraydon reference does not teach that when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from Rename 2 to GPR.

In light of the arguments set forth above, Applicants submit that the Faraydon reference fails to teach or suggest all of the limitations of independent claims 1, 10 and 19. Claim 4, 13 and 20, which depend on independent claims 1, 10 and 19, respectively, are not rendered obvious over the cited prior art reference. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 4, 13 and 20 under 35 U.S.C. §103(a).

Claim Rejections - 35 U.S.C. § 103

Claims 6 and 15 are rejected under 35 U.S.C. § 103(a) as unpatentable over Faraydon in view of U.S. Patent No. 5, 546,554 ("Yung"). Applicants respectfully traverse the rejection for the following reasons.

Claim 6 and 15 depend on independent claims 1 and 10, respectively. Applicants respectfully submit that the cited prior art references fail to teach or suggest all of the limitations of independent claims 1 and 10. Applicants submit that Faraydon and Yung fail to teach that *when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure*, as recited in claims 1 and 10.

Yung teaches a dynamic register management in a floating point unit. Yung is cited by the Examiner to provide teachings for the subject matter added in claims 6 and 15, which relates to flushing the contents of the assigned available physical registers from the assigned available physical registers. Yung, however, does not teach that when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure, as recited in claims 1 and 10.

In light of the arguments set forth above, Applicants submit that Faraydon and Yung fail to teach or suggest all of the limitations of independent claims 1 and 10. Claim 6 and 15, which depend on independent claims 1 and 10, respectively, are not rendered obvious over the cited prior art references. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 6 and 15 under 35 U.S.C. §103(a).

Claim Rejections - 35 U.S.C. § 103

Claims 9 and 18 are rejected under 35 U.S.C. § 103(a) as unpatentable over Faraydon in view of Tanebaum, Structured Computer Organization, 2nd Edition, 1984, page 11 ("Tanebaum"). Applicants respectfully traverse the rejection for the following reasons.

Claim 9 and 18 depend on independent claims 9 and 18, respectively.

Applicants respectfully submit that the cited prior art references fail to teach or suggest all of the limitations of independent claims 1, 10 and 19. Applicants submit that Faraydon and Tanebaum fail to teach that *when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure*, as recited in claims 1 and 10.

Tanebaum is cited by the Examiner to provide teachings for the subject matter added in claims 9 and 18, which relates to software performing the method recited in claims 1 and 10. Tanebaum, however, does not teach that when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure, as recited in claims 1 and 10.

In light of the arguments set forth above, Applicants submit that the Faraydon and Tanebaum references fail to teach or suggest all of the limitations of independent claims 1 and 10. Claim 9 and 18, which depend on independent claims 1 and 10, respectively, are not rendered obvious over the cited prior art references. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 9 and 18 under 35 U.S.C. §103(a).

CONCLUSION

In view of the remarks set forth above, Applicant contends that Claims 1-20 are presently pending in this application, are patentable and in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

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Respectfully submitted,

By_____

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